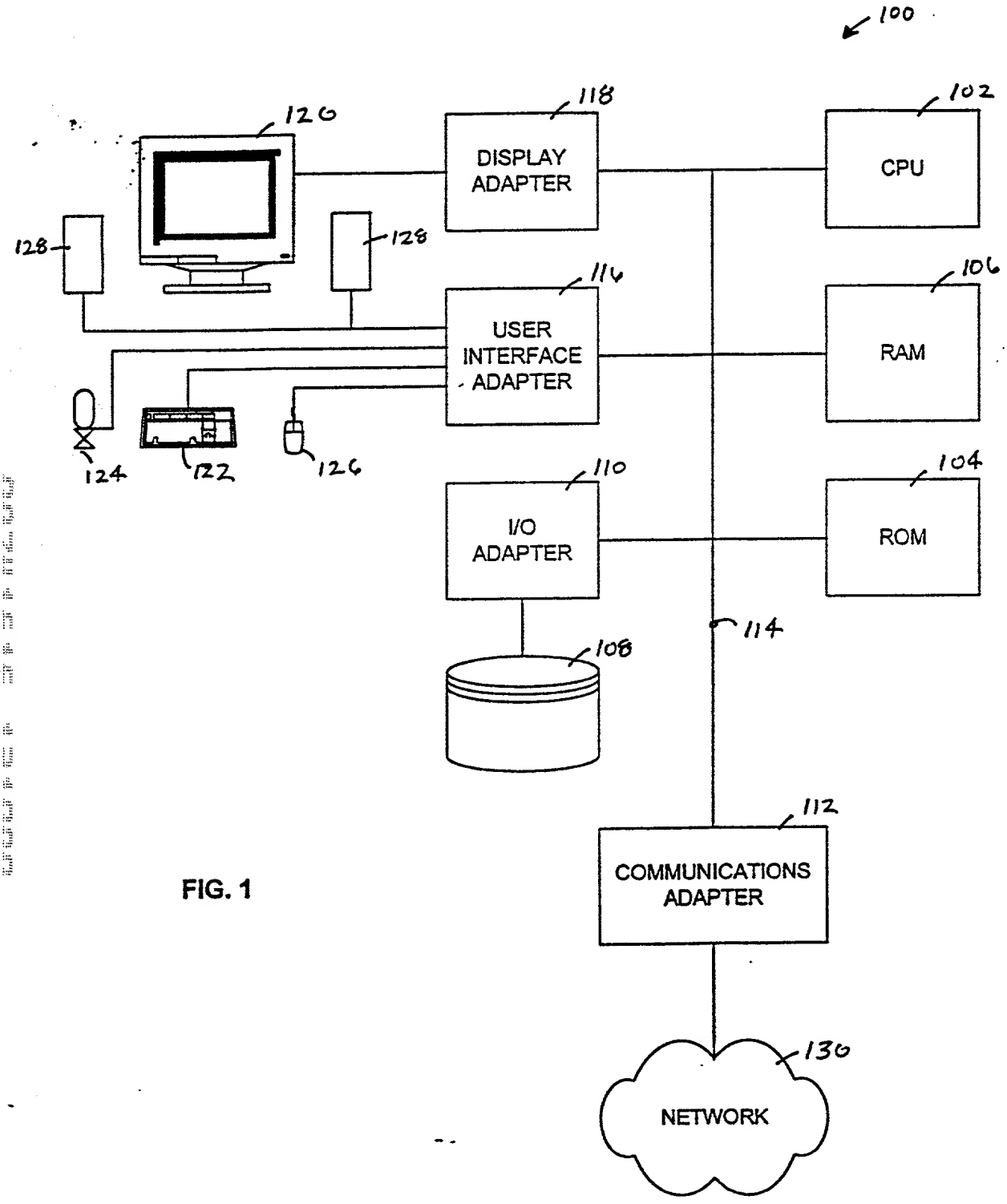
100
118
DISPLAY ADAPTER
102
CPU
120
128
128
116
USER INTERFACE ADAPTER
106
RAM
124
122
126
110
I/O ADAPTER
104
ROM
114
108
112
COMMUNICATIONS ADAPTER
130
NETWORK

FIG. 1

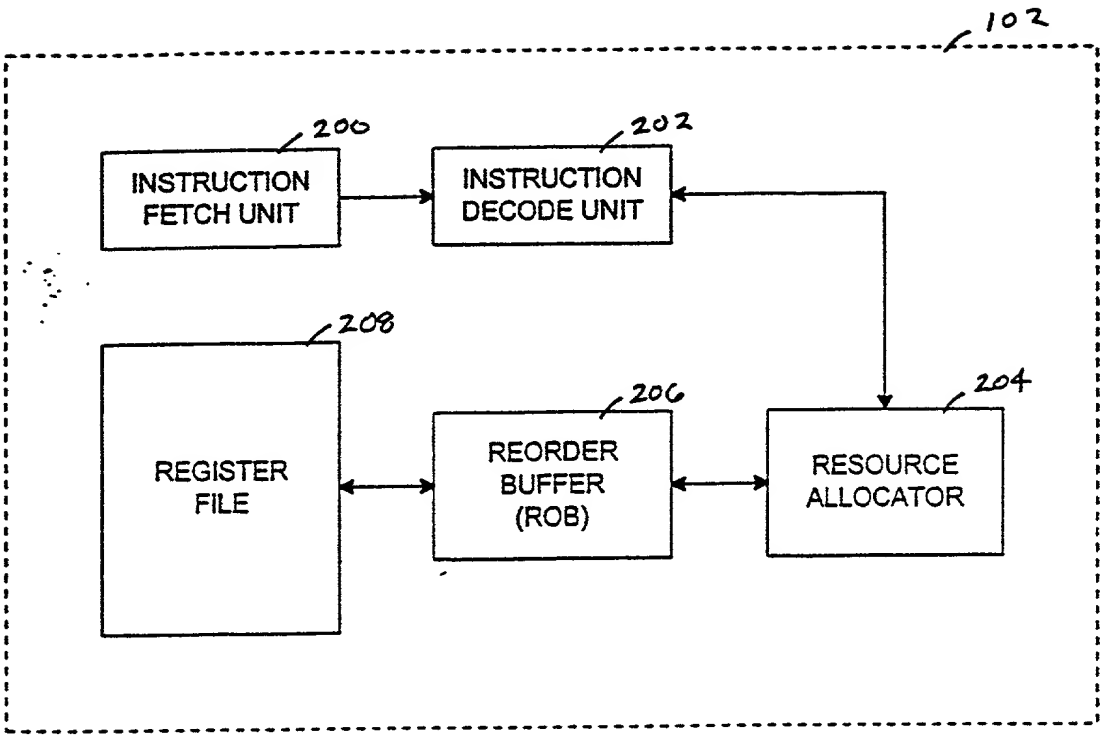
102
200
INSTRUCTION FETCH UNIT
202
INSTRUCTION DECODE UNIT
208
REGISTER FILE
206
REORDER BUFFER (ROB)
204
RESOURCE ALLOCATOR

FIG. 2

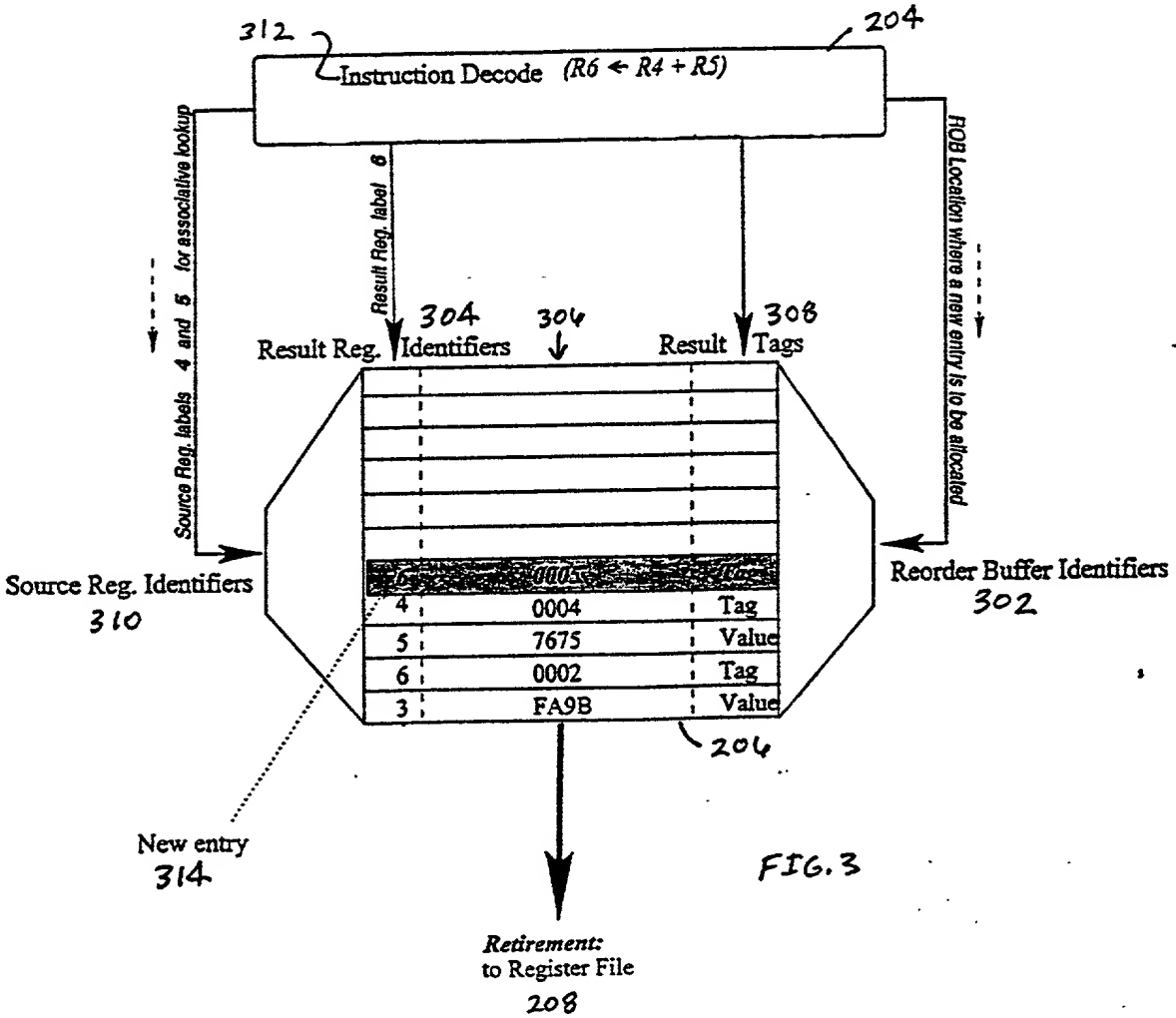
312
204
Instruction Decode (R6 ← R4 + R5)
Result Reg. label 6
ROB Location where a new entry is to be allocated
Source Reg. labels 4 and 5 for associative lookup
304
304
308
Result Reg. Identifiers
Result Tags
Source Reg. Identifiers
310
Reorder Buffer Identifiers
302
4 0004 Tag
5 7675 Value
6 0002 Tag
3 FA9B Value
206
New entry
314
Retirement:
to Register File
208

FIG. 3

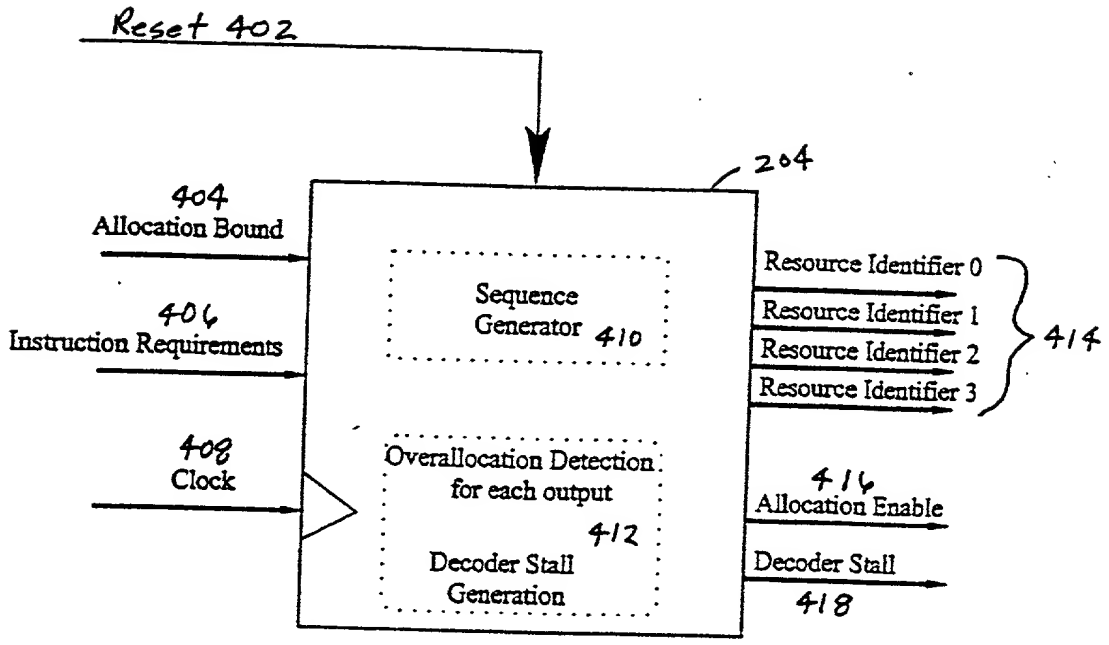
Reset 402
204
404
Allocation Bound
406
Instruction Requirements
408
Clock
Sequence Generator 410
Overallocation Detection for each output
412
Decoder Stall Generation
Resource Identifier 0
Resource Identifier 1
Resource Identifier 2
Resource Identifier 3
414
416
Allocation Enable
Decoder Stall
418

FIG. 4a

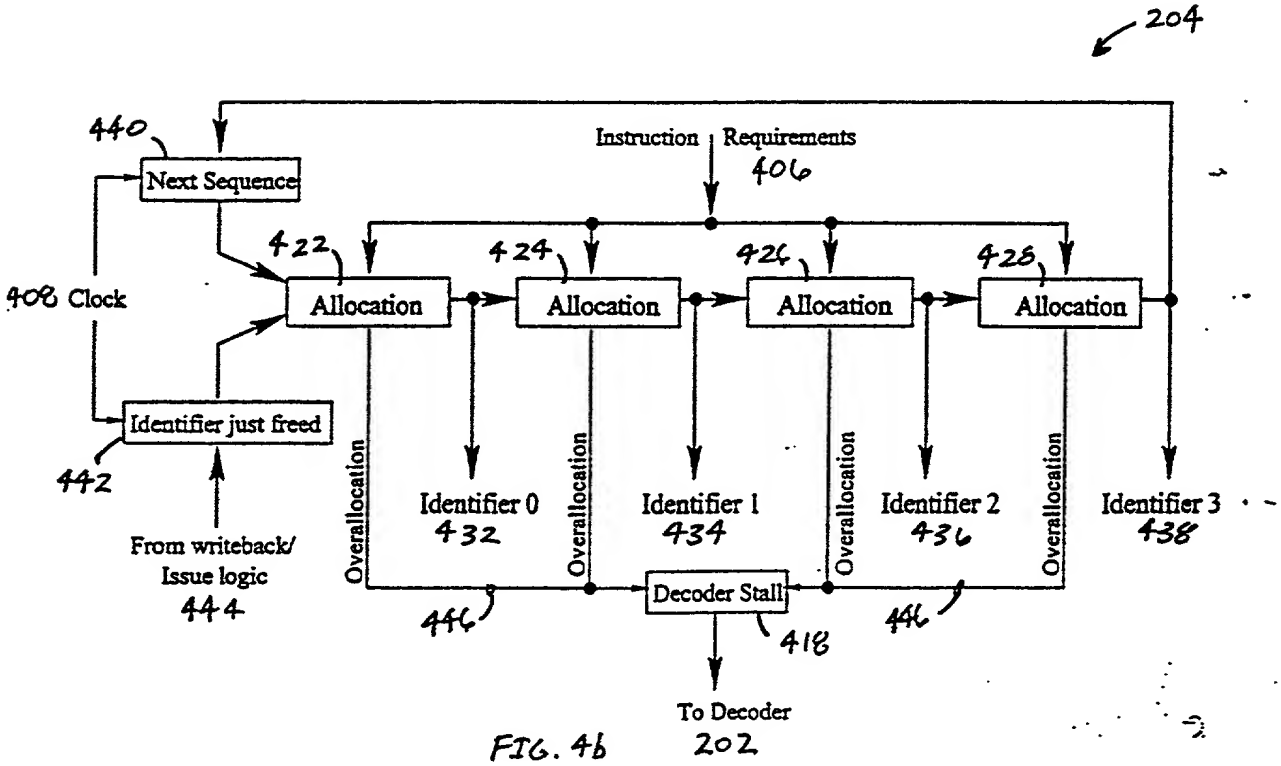
204
440
Next Sequence
Instruction Requirements
406
422
424
426
428
408 Clock
Allocation
Allocation
Allocation
Allocation
Identifier just freed
442
From writeback/ Issue logic
444
Overallocation
Identifier 0
432
Overallocation
Identifier 1
434
Overallocation
Identifier 2
436
Overallocation
Identifier 3
438
446
Decoder Stall
418
446
To Decoder
202

FIG. 4b

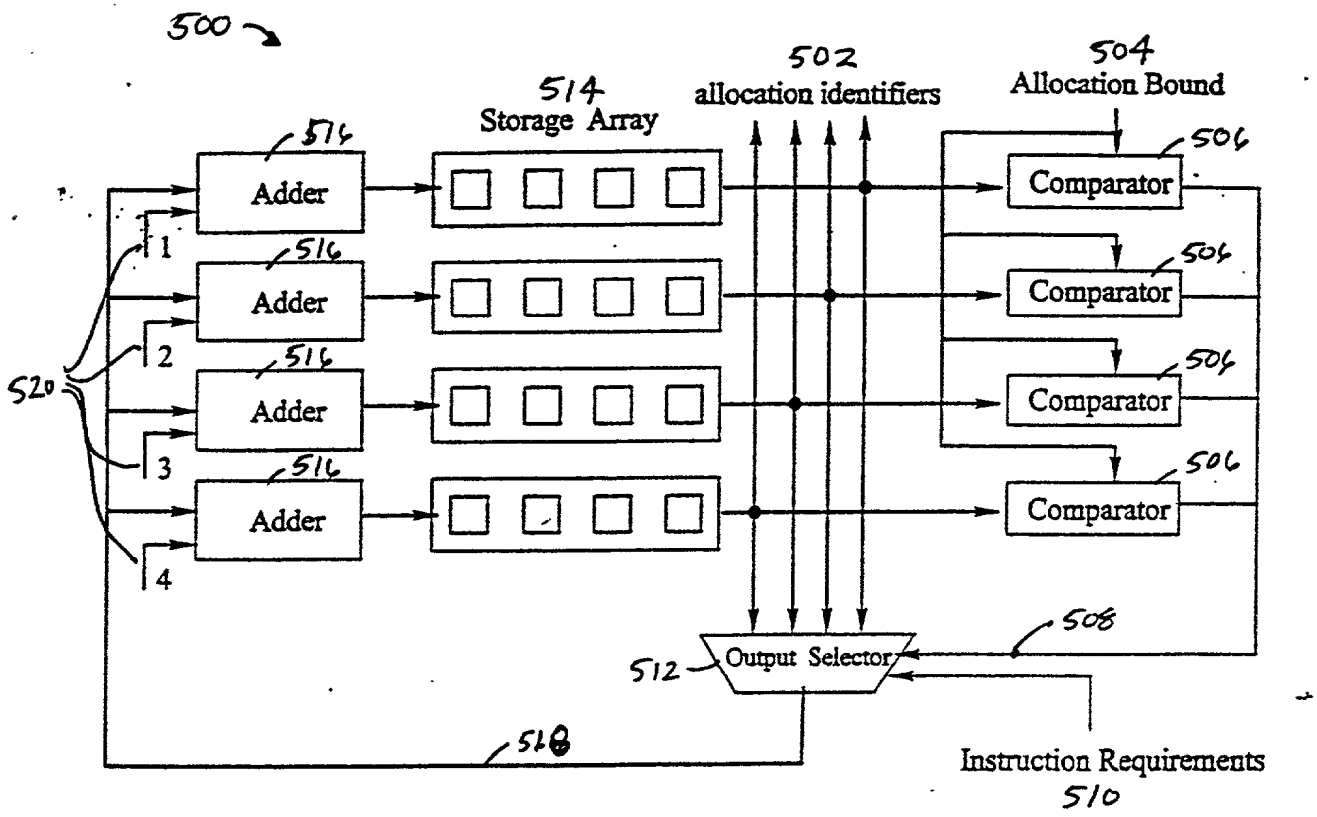
500
514
Storage Array
502
allocation identifiers
504
Allocation Bound
516
Adder
506
Comparator
1
2
3
4
520
512
Output Selector
508
518
Instruction Requirements
510

FIG. 5

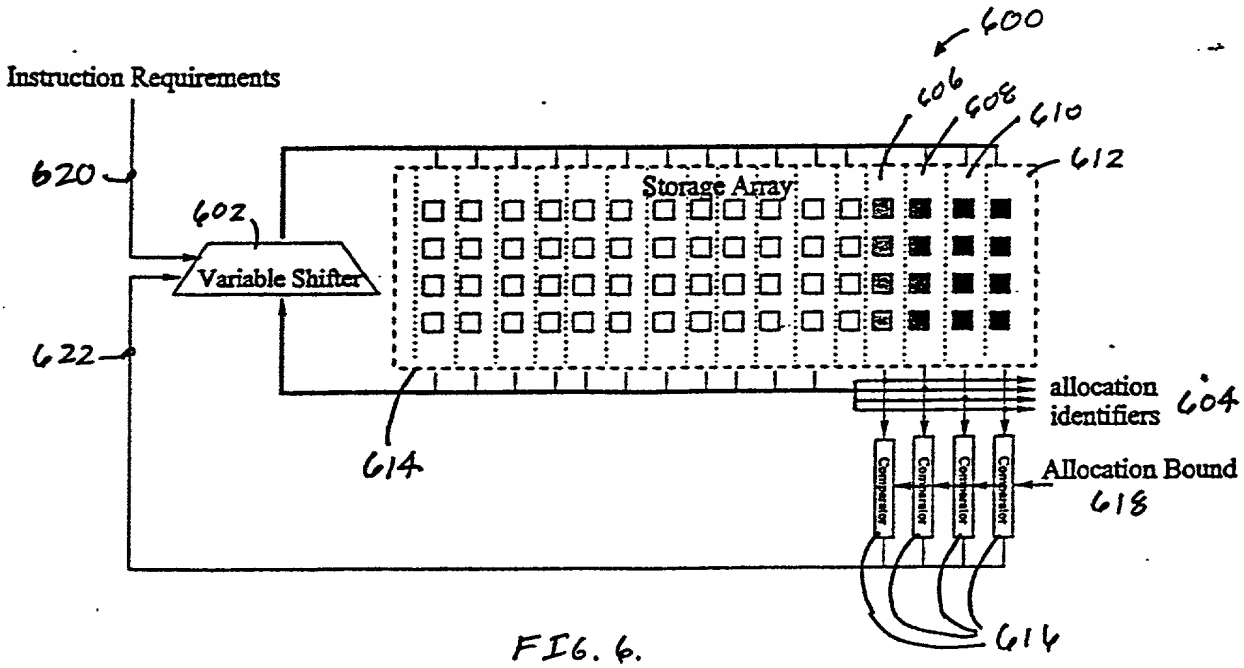
600
Instruction Requirements
606
608
610
612
620
602
Variable Shifter
Storage Array
622
allocation identifiers
604
614
Comparator
Allocation Bound
618
614

FIG. 6.

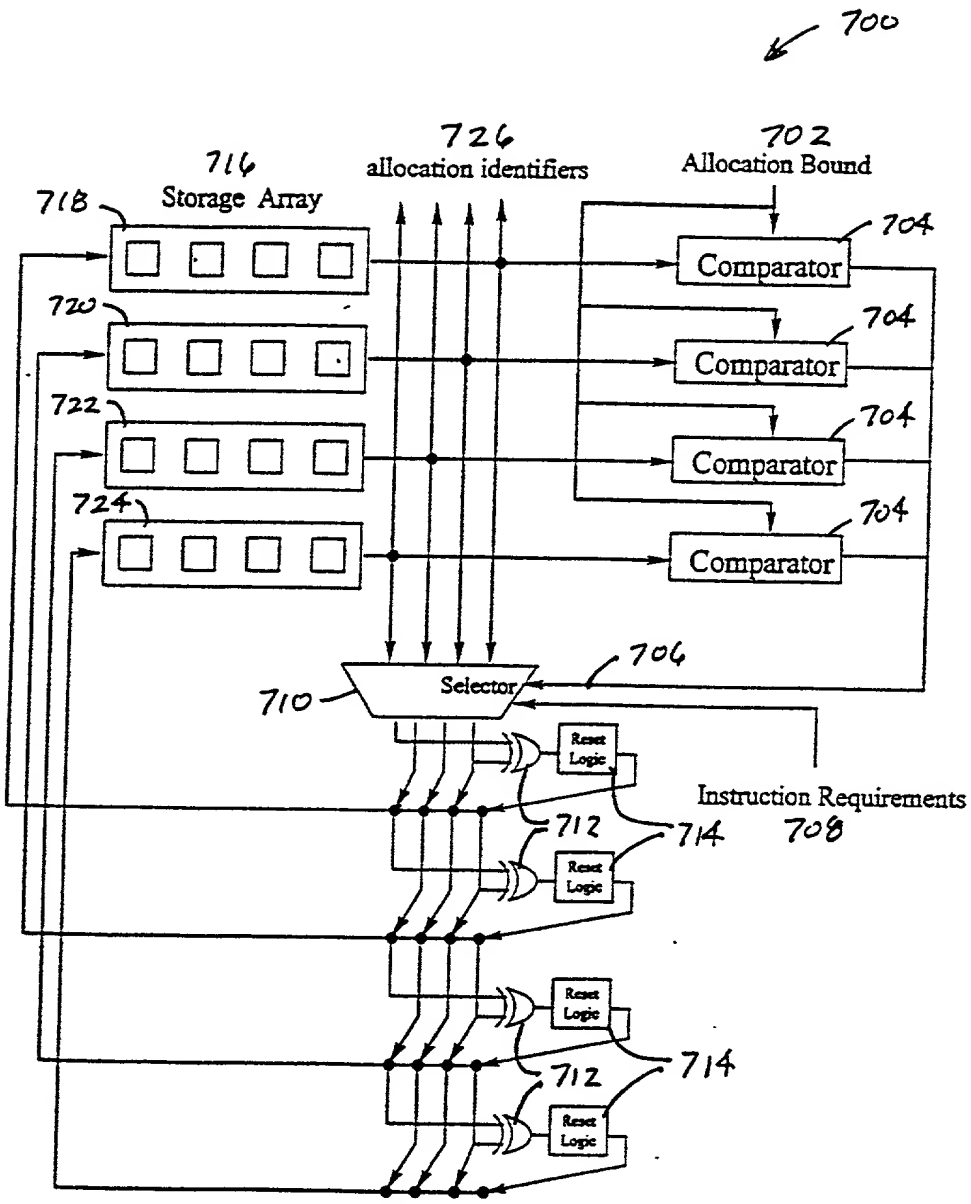
700
726
allocation identifiers
702
Allocation Bound
716
Storage Array
718
720
722
724
Comparator
704
Selector
706
710
Reset Logic
712
714
Instruction Requirements
708

FIG. 7

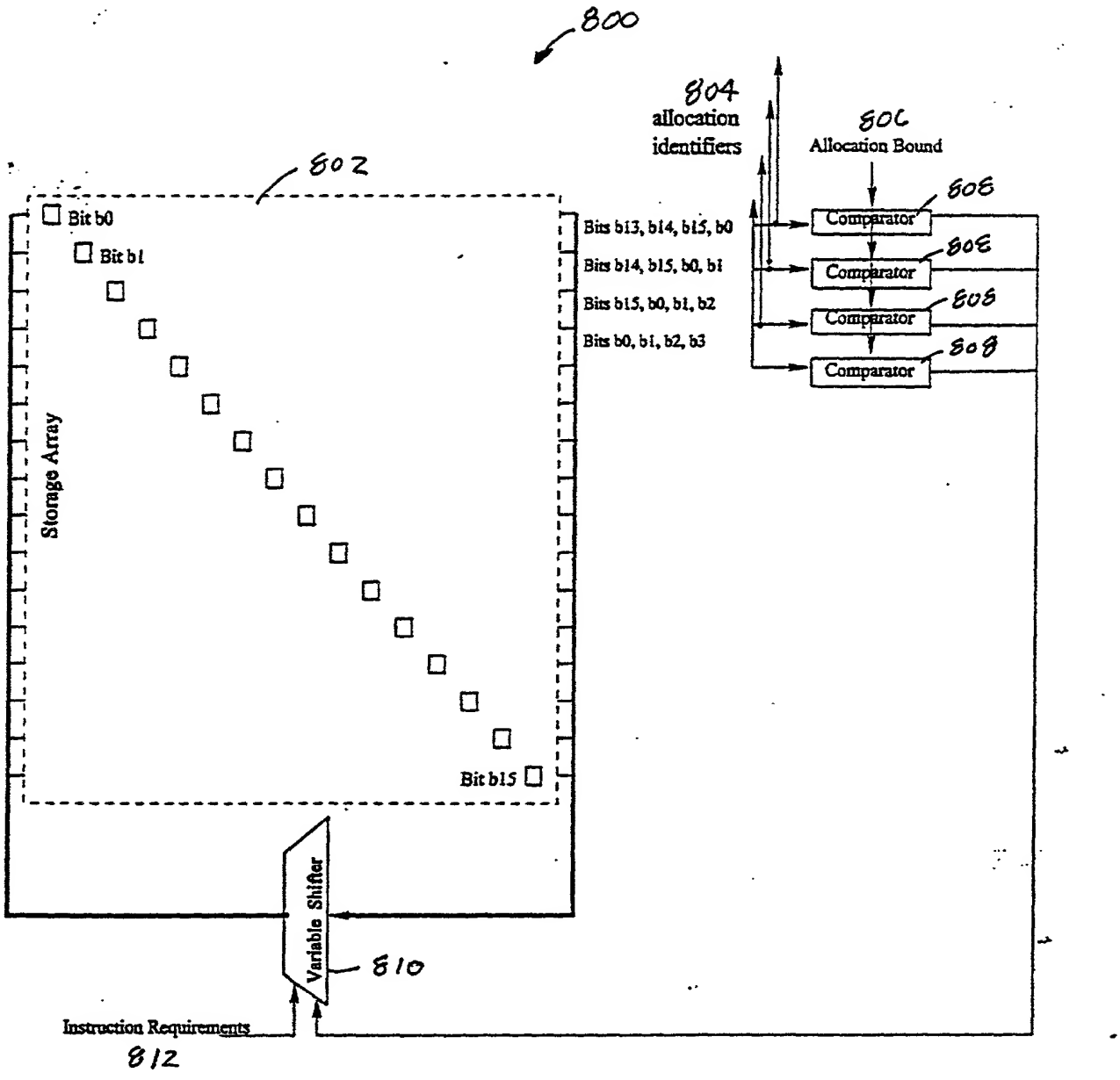
800
804
allocation identifiers
806
Allocation Bound
802
Bit b0
Bit b1
Bit b15
Storage Array
Bits b13, b14, b15, b0
Bits b14, b15, b0, b1
Bits b15, b0, b1, b2
Bits b0, b1, b2, b3
Comparator
Comparator
Comparator
Comparator
808
Variable Shifter
810
Instruction Requirements
812

FIG. 8

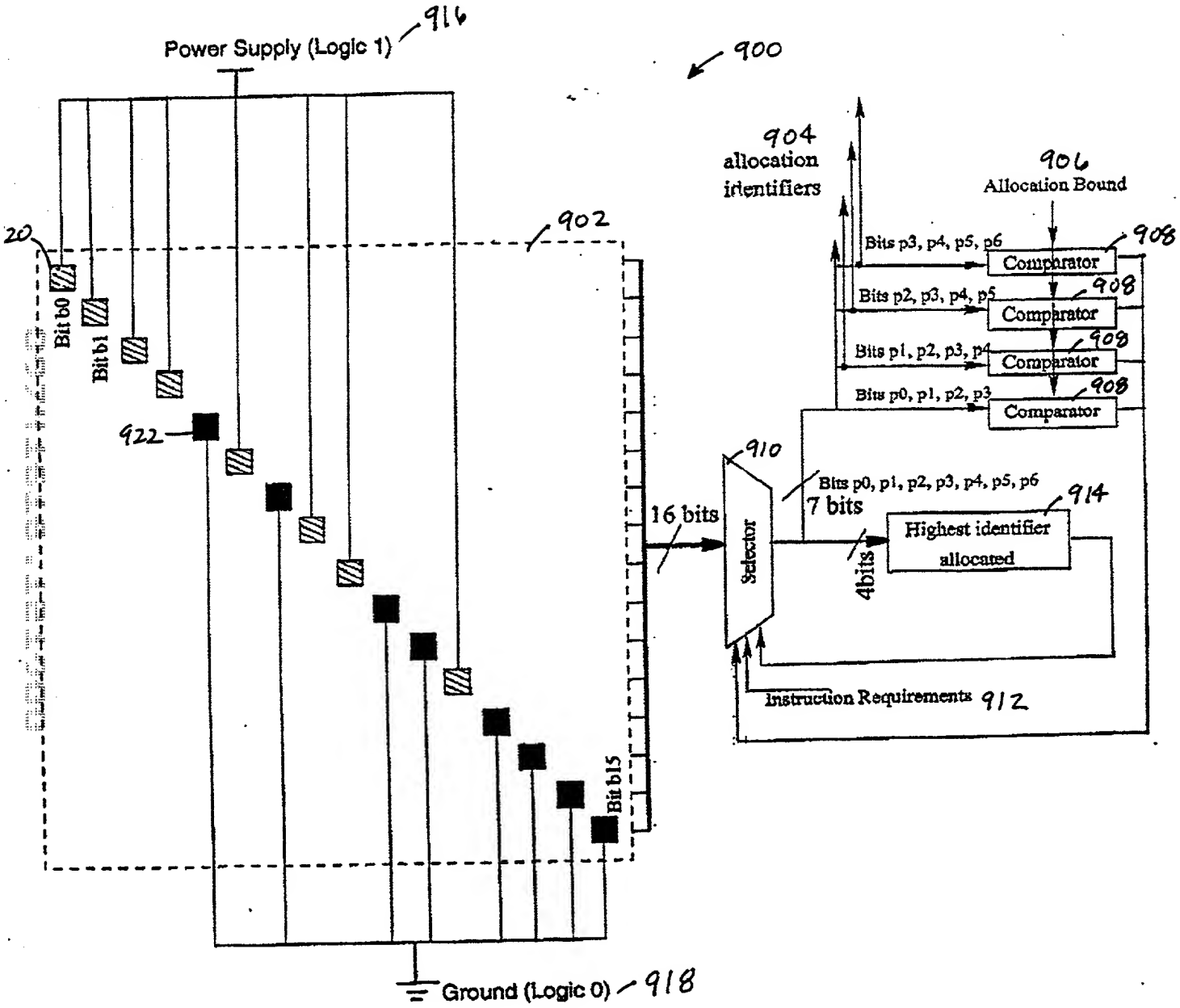
916
Power Supply (Logic 1)
900
904
allocation identifiers
906
Allocation Bound
902
20
Bit b0
Bit b1
922
Bits p3, p4, p5, p6
Comparator
908
Bits p2, p3, p4, p5
Comparator
908
Bits p1, p2, p3, p4
Comparator
908
Bits p0, p1, p2, p3
Comparator
908
910
Bits p0, p1, p2, p3, p4, p5, p6
7 bits
914
16 bits
Selector
Highest identifier allocated
4bits
Instruction Requirements 912
Bit b15
Ground (Logic 0)
918

FIG. 9

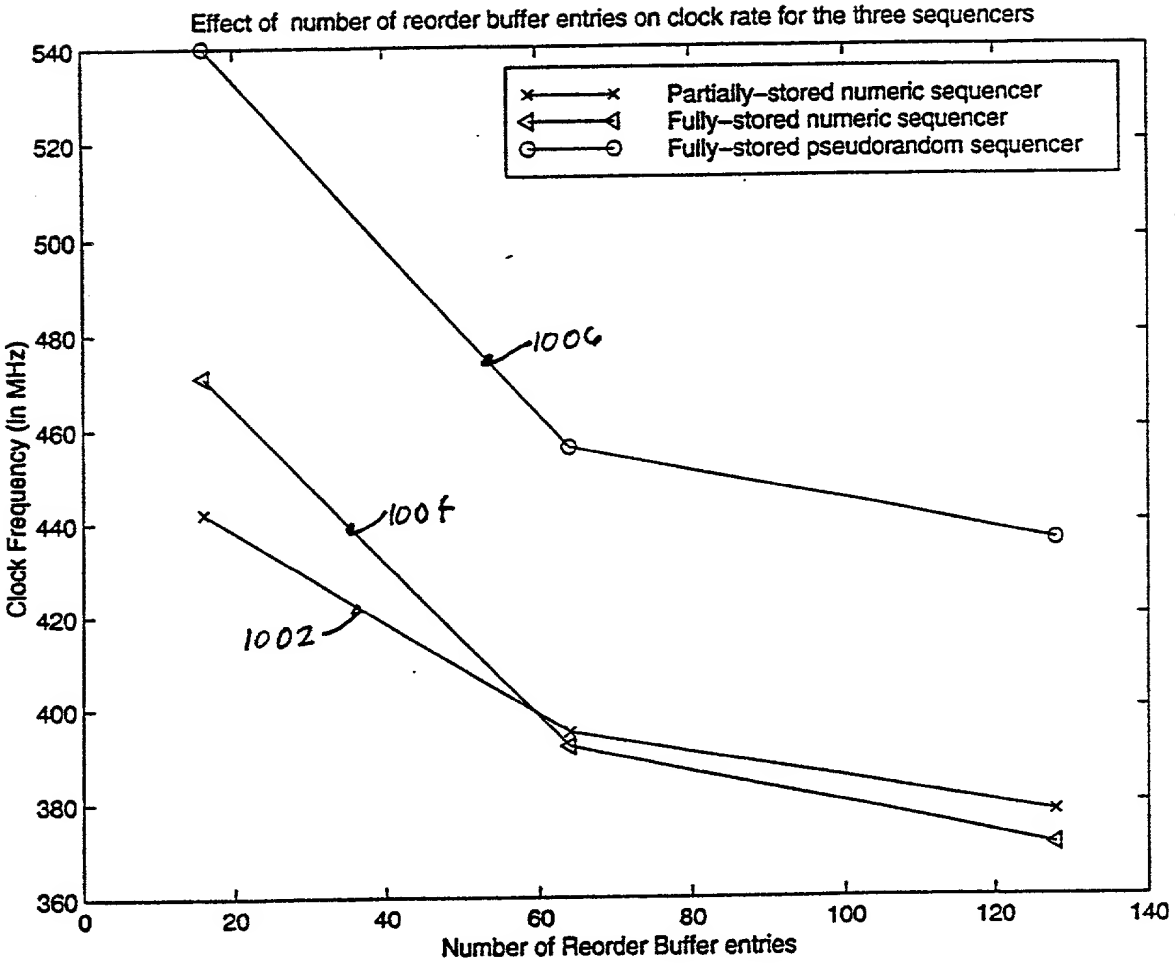

Figure 10: Effect of number of reorder buffer entries on clock rate for the three sequencers